REMARKS

Amended Claims

Claims 4, 6-9, 13, 15, 19, 25, 27, 38, and 40 are amended herein.

In the Specification

The Examiner objected to claim 4, stating that "[c]laim 4 recites: 'the select gate' which lacks a clear antecedent basis. It is clear from the detailed description that the select gate derives an antecedent basis from select gate (610), and not from the 'a select gate memory cell (610)' as claimed." Claim 4 is amended herein to change "a select gate memory cell" to "a select gate" to correct this typographical error in claim 4 and provide the antecedent basis. Applicant contends the typographical error is apparent from the context of the detailed description and claims, as noted by the Examiner. As such, Applicant respectfully contends that the correction does not comprise new matter and therefore requests withdrawal of the Examiner's objection to claim 4 and the specification.

Claim Objections

Claims 1, 12-18, 25, 27 and 40 were objected due to informalities. Applicant traverses this objection and maintains that claims 1, 12-18, 25, 27 and 40 are allowable for the following reasons:

In objecting to claims 1, 12-18, 25, 27 and 40, the Examiner stated that "[e]ach of these claims either recites: 'memory array formed on a substrate' or 'forming two raised areas on a substrate'; however, it is clear from the detailed description that the respective elements are formed in a substrate (paragraph [0049]: 'In creating the vertical NOR architecture memory cell structure 604 a trench 630 is formed in a substrate 608', paragraph [0071]: 'a series of substrate pillars 828 are formed in a substrate 808 with trenches 830 located between them'). Appropriate correction is required."

Applicant respectfully disagrees with the Examiner maintains that claims 1, 12-18, 25, 27 and 40 are not informal or inconsistent with the detailed description.

Applicant respectfully maintains that the act of forming a structure in a substrate by the removal of substrate material would be viewed as equivalent to forming a structure on a substrate by the deposition of substrate material by one of ordinary skill in the art. Applicant notes that [0030] of the Present Application states, in part, "The terms wafer and substrate used previously

and in the following description include any base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the claims and equivalents thereof." Applicant observes that in this, at least, silicon-on-sapphire (SOS) technology and silicon-on-insulator (SOI), both refer to the forming of a structure on a base semiconductor.

Applicant also notes that the specification does describe the forming of structures "on a substrate" in, at least, Paragraphs [0014], [0016], [0019], and [0030] of the Present Application. Applicant further notes that the claims as originally filed are part of the disclosure and respectfully maintains that claims 1, 12-18, 25, 27 and 40 as filed describe the forming of structures "on a substrate", and as such Applicant is allowed to rely on them as part of the original disclosure. *See*, MPEP §608.01(l) ("In establishing a disclosure, applicant may rely not only on the description and drawing as filed but also on the original claims if their content justifies it.")

As such, Applicant asserts that the relevant features of claims 1, 12-18, 25, 27 and 40, in particular, the forming of structures "on a substrate", have been described in the specification in such a way as to enable one skilled in the art to practice the invention, and therefore contends claims 1, 12-18, 25, 27 and 40 are not informal. Applicant therefore respectfully requests reconsideration and withdrawal of the objections to the claims by the Examiner.

In the Drawings

The drawings were also objected to under 37 CFR 1.83(a), as the drawings must show every feature of the invention specified in the claims. Applicant respectfully traverses this objection.

The Examiner stated that "[t]he drawings must show every feature specified in the claims. Therefore the "on the substrate" and "depositing additional substrate material on the substrate" in "forming two pillars on a substrate further comprises depositing additional substrate

material on the substrate to form the two pillar" of claim 18 must be shown or the feature(s) canceled from the claim(s)." (Office Action mailed September 22, 2005, Page 3)

Applicant disagrees with the Examiner and believes that no further drawings are required under 37 CFR 1.83(a). Applicant respectfully maintains, as detailed above, that the act of forming a structure in a substrate by the removal of substrate material would be viewed as equivalent to forming a structure on a substrate by the deposition of substrate material by one of ordinary skill in the art. Applicant also notes that the specification does describe the forming of structures "on a substrate" in, at least, Paragraphs [0014], [0016], [0019] and [0030] of the Present Application.

As such, Applicant respectfully maintains that the Figures of the Present Application do show all claimed features in that they detail a substrate having structures formed on/in the substrate at various intermediate stages of the manufacturing process. Applicant in particular notes that the forming of pillars on a substrate are shown in, at least, Figures 8B and 8C and described in Paragraphs [0071], [0073]-[0075], [0053]-[0054], [0061]-[0064], and [0066]. *See also*, Present Application, Figures 8A-8C, 6A-6B, 7A and 7C; Paragraphs [0071]-[0078], [0049]-[0055], [0061]-[0064], and [0066]-[0067].

Applicant also respectfully submits that drawings are not required for process claims for, as stated in MPEP §601.01(f), "[i]t has been USPTO practice to treat an application that contains at least one process or method claim as an application for which a drawing is not necessary for an understanding of the invention under 35 U.S.C. 113 (first sentence)."

The Applicant therefore requests removal of the objections to the drawings by the Examiner under 37 CFR 1.83(a) because the Figures of the Present Application do show all claimed features of claim 18. The Applicant also requests approval of the formal drawings.

Claim Rejections Under 35 U.S.C. § 103

Claims 4-12, 15-30 and 32-40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,888,868 in view of Sakui et al. (U.S. Patent Application No. 2001/0038118). Claims 4-12, 15-30 and 32-40 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,888,868) in view of Takahashi et al. (U.S. Patent Application No. 2003/0209767). Applicant respectfully traverses these rejections and submits that claims 4-12, 15-30 and 32-40 are allowable for the following reasons.

Applicant respectfully maintains that Yamazaki et al. discloses a memory array of NAND memory cell strings having select gates and floating gate memory cells formed vertically and does not disclose or suggest an NROM memory cell structure having a substrate, comprising two raised areas, defining a trench therebetween; an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of the trench; a select gate, wherein the select gate is formed vertically on a second sidewall of the trench a first bitline, wherein the first bitline is coupled to a drain of the select gate; and a second bitline, wherein the second bitline is coupled to a source/drain of the NROM memory cell. *See*, Yamazaki et al., Figures 8F-8H; Abstract; Column 10, Line 43 to Column 11, Line 39. Applicant therefore respectfully submits that Yamazaki et al. fails to teach or disclose all elements of the Applicant's claimed invention.

In addition, Applicant respectfully maintains that Sakui et al. discloses a memory array of NAND memory cell strings having memory cells and select gates formed vertically with common control gates and does not disclose or suggest an NROM memory cell structure having a substrate, comprising two raised areas, defining a trench therebetween; an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of the trench; a select gate, wherein the select gate is formed vertically on a second sidewall of the trench a first bitline, wherein the first bitline is coupled to a drain of the select gate; and a second bitline, wherein the second bitline is coupled to a source/drain of the NROM memory cell. *See*, Sakui et al., Abstract and Summary. Applicant therefore respectfully submits that combining the elements of Yamazaki et al. with Sakui et al. also fails to teach or disclose all elements of the Applicant's claimed invention, either alone or in combination.

Applicant also respectfully maintains that Takahashi et al. discloses a memory array of memory cells formed vertically in trenches with bit lines diffused at the top and bottom of the trenches and does not disclose or suggest an NROM memory cell structure having a substrate, comprising two raised areas, defining a trench therebetween; an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of the trench; a select gate, wherein the select gate is formed vertically on a second sidewall of the trench a first bitline, wherein the first bitline is coupled to a drain of the select gate; and a second bitline, wherein the second bitline is coupled to a source/drain of the NROM memory cell. *See*, Takahashi et al., Figure 3, Abstract, and Summary. Applicant therefore respectfully submits that combining the elements of Yamazaki et al. with Takahashi et al. also fails to teach or disclose all elements of the Applicant's claimed invention, either alone or in combination.

Applicant's claim 4 recites, in part, "a substrate, comprising two raised areas, defining a trench therebetween; an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of the trench; a select gate, wherein the select gate is formed vertically on a second sidewall of the trench" and "a first bitline, wherein the first bitline is coupled to a source/drain of the select gate; and a second bitline, wherein the second bitline is coupled to a source/drain of the NROM memory cell." As detailed above, Applicant submits that Yamazaki et al. and Sakui et al. or Yamazaki et al. and Takahashi et al. fail to teach or disclose such an NROM memory cell structure, either alone or in combination. As such, both Yamazaki et al. and Sakui et al. or Yamazaki et al. and Takahashi et al. fail to teach or disclose all elements of claim 4.

Applicant's claim 7 recites, in part, "a substrate, comprising a plurality of pillars and associated intervening trenches; a plurality of memory cell structures, each memory cell structure comprising, an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of a trench, a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the NROM memory cell by a source/drain region formed at the bottom of the trench" and "at least one first bitline, wherein the at least one first bitline is coupled to one or more select gate source/drain regions formed at the top of the plurality of pillars of the plurality of memory cell structures; and at least one second bitline, wherein the at least one second bitline is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of memory cell structures." As detailed above, Applicant submits that Yamazaki et al. and Sakui et al. or Yamazaki et al. and Takahashi et al. fail to teach or disclose such an NROM memory array, either alone or in combination. As such, both Yamazaki et al. and Sakui et al. or Yamazaki et al. and Takahashi et al. fail to teach or disclose all elements of claim 7.

Applicant's claim 15 recites, in part, "forming two raised areas on a substrate, the raised areas defining an associated intervening trench; forming an NROM memory cell on a first sidewall of the trench; forming a select gate on a second sidewall of the trench; forming a source/drain region at the bottom of the associated intervening trench; forming source/drain regions on the top of the two raised areas" and "forming a first bitline, wherein the first bitline is coupled to a source/drain of the select gate; and forming a second bitline, wherein the second bitline is coupled to a source/drain of the NROM memory cell." As detailed above, Applicant submits that Yamazaki et al. and Sakui et al. or Yamazaki et al. and Takahashi et al. fail to teach or disclose such a method of forming an NROM memory cell structure, either alone or in

combination. As such, both Yamazaki et al. and Sakui et al. or Yamazaki et al. and Takahashi et al. fail to teach or disclose all elements of claim 15.

Applicant's claim 25 recites, in part, "forming a plurality of pillars and associated intervening trenches on a substrate by depositing a layer of masking material, patterning the masking material, and anisotropically etching the substrate; forming a plurality of NROM memory cell structures, each NROM memory cell structure having a trapping layer and a coupled select gate" and "forming at least one first bitline, wherein the at least one first bitline is coupled to one or more select gate source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures; and forming at least one second bitline, wherein the at least one second bitline is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures." As detailed above, Applicant submits that Yamazaki et al. and Sakui et al. or Yamazaki et al. and Takahashi et al. fail to teach or disclose such a method of forming a floating gate memory array, either alone or in combination. As such, both Yamazaki et al. and Sakui et al. or Yamazaki et al. and Takahashi et al. fail to teach or disclose all elements of claim 25.

Applicant's claim 27 recites, in part, "forming a plurality of pillars and associated intervening trenches on a substrate; and forming a plurality of NROM memory cell structures, each NROM memory cell structure is formed by, forming an NROM memory cell on a first sidewall of a trench; forming a select gate on a second sidewall of the trench; and forming a source/drain region at the bottom of the trench; forming at least one first bit/data line, wherein the at least one first bit/data line is coupled to one or more select gate source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures; and forming at least one second bit/data line, wherein the at least one second bit/data line is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures." As detailed above, Applicant submits that Yamazaki et al. and Sakui et al. or Yamazaki et al. and Takahashi et al. fail to teach or disclose such a method of forming an NROM memory array, either alone or in combination. As such, both Yamazaki et al. and Sakui et al. or Yamazaki et al. and Takahashi et al. fail to teach or disclose all elements of claim 27.

Applicant's claim 40 recites, in part, "forming a plurality of pillars and associated intervening trenches on a substrate; forming a plurality of NROM memory cells on a first sidewall of each trench; forming a plurality of select gates on a second sidewall of each trench;

forming one or more source/drain regions on the top of the plurality of pillars and at the bottom of the associated intervening trenches," and "forming at least one first bitline, wherein the at least one first bitline is coupled to one or more select gate source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures; and forming at least one second bitline, wherein the at least one second bitline is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures." As detailed above, Applicant submits that Yamazaki et al. and Sakui et al. or Yamazaki et al. and Takahashi et al. fail to teach or disclose such a method of forming an NROM EEPROM memory device, either alone or in combination. As such, both Yamazaki et al. and Sakui et al. or Yamazaki et al. and Takahashi et al. fail to teach or disclose all elements of claim 40.

Applicant respectfully contends that claims 4, 7, 15, 25, 27, and 40 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 5-6, 8-12, 16-24, 26, 28-30 and 32-39 depend from and further define claims 4, 7, 15, 25, 27, and 40, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) and allowance of claims 4-12, 15-30 and 32-40.

Allowable Subject Matter

Applicant thanks the Examiner for the indication of allowability for claims 1-3 and 13-14. Applicant notes that claim 13 was amended to correct a typographical error, changing "select gate drain" to "select gate source/drain." Applicant contends the typographical error is apparent from the context of the detailed description and claims and therefore requests approval of the change to allowed claim 13.

Claim 31was objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Applicant thanks the Examiner for this indication. However, as detailed above, claim 27 has been shown to be patentably distinct from the cited reference. Applicant respectfully contends that, as claim 31 depends from and further defines claim 27, it is also considered to be in condition for allowance. Applicant thus respectfully requests reconsideration and withdrawal of the objection, and allowance of claim 31.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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